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09/732,570	12/08/2000	Mark Steven Boggs	99P07535 US04	6769

7590 06/02/2004

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EXAMINER	
KANG, INSUN	
ART UNIT	**PAPER NUMBER**
2124	8

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/732,570	BOGGS ET AL.	
	Examiner	Art Unit	
	Insun Kang	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *52-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *52-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed 3/10/2004.

2. As per applicant's request, claims 54-59, 61 and 62 have been amended. Claims 52-62 are pending in the application.

Claim Objections

3. The objections of claims 54, 56 and 61 have been withdrawn due to the corrections of the claims.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 60 and 61 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. The rejections of claims 59 and 62 under 35 U.S.C. 112, second paragraph, have been withdrawn due to the corrections of the claims. The limitation "said instruction" in line 30 of claim 59 has been corrected as "said program." However, the rejections of dependent claims 60 and 61 are maintained due to the dependency on the amended parent claim 59. Claim 60 recites the limitation "said instructions" in lines 2, page 4. There is insufficient antecedent basis for this limitation in the claim. The sentence "said instructions" in line 2, page 4 is interpreted as "said instruction." Appropriate correction is required.

Regarding claim 61, this claim is objected for dependency on the above rejected parent claim 60.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 52-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roy et al. (US Patent 6,321,331), hereinafter referred to as "Roy," in view of Logan III et al. (US Patent 6,243,857), hereinafter referred to as "Logan."

Regarding claim 52, Roy discloses a method for debugging a program in real time and while said program is executed ("A widely used technique for debugging a program which is running in real time is called "tracing." Tracing involves recording the transactions performed by the computer as it executes the program code," Roy, col 1, lines 28-34; "the contents of the event history buffer can be recorded over time by the diagnostic device to provide a real time record of the processing events occurring in the chip during real time. This real time record taken together with knowledge of the program code being executed provides a true picture of the processors' execution sequence in real time and thereby expedite debugging of code," Roy, col 3, lines 52-59; see also col 3, lines 13-32; col 7, lines 45-54).

Roy, however, does not disclose that the program is executed by a programmable logic controller. Logan discloses a programmable logic controller ("a manually-derived flowchart was converted to a ladder diagram which was then programmed into a programmable controller

controlled a machine via an I/O device that produced the requisite signals for machine control," col 6, lines 18-42, lines 59-65) to automate monitoring and controlling of execution.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate the teaching of Logan to the method of Roy. One having ordinary skill would have been motivated to include the programmable logic controller to gain control of machinery in flexible automation schemes and to control essentially independent sequential processes at the same time (with ladder diagram).

Also, Roy does not disclose displaying a section of said program indicated by a user to be debugged. However, Logan discloses displaying a section of said program indicated by a user to be debugged ("a feature of display so as to alert the user quickly and to provide accurate change identification," col 5, lines 25-67; "the debugger...is supplied with data...in which when an interrupt is inputted via the keypad...providing data to the debugger to indicated which block or blocks are being executed at the time of interrupt. Inhibit signals come from the keyboard 92...The Debugger...drives **the display to highlight the particular block which was executing at the time of interrupt...The block numbers are displayed for purpose of enabling the programmer to get back into the flowchart at the required spot and highlights are utilized to indicate, during an interrupt cycle, which blocks in the program were executing at the time of the interrupt...only the flowcharts that are necessary to be edited will be called up to the display**," col 5 lines 25-col 6 lines 17). This feature of display "provides for ease of editing...with the debugging unit providing for ease of debugging an original program during a run-time execution of the program (col 3, lines 57-67; col 4, lines 37-67)."

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Logan to the method of Roy. One skilled in the art would have been motivated to include the feature of display for the purpose of ease editing and debugging on the fly as suggested by Logan (col 3, lines 57-67; col 4, lines 37-67; col 5 lines 25-col 6 lines 17).

Roy further discloses saving original compiled code of the program ("...debugging computer which preferably has a copy of the program code stored therein," "The information collected by the computer 44 is associated with each line of code being executed by the ASIC by stepping through the copy of the code which is stored in the computer 44," col 7, lines 21-54; see also col 3, lines 1-32; col 4, lines 15-20); compiling said section of said program to be debugged in another section of memory (col3, lines 14-59; col 4 lines 1-56); jumping to said another section of said memory during execution of said program when an instruction indicated to be debugged is to be executed (col 3, lines 1-42; col 4, lines 51-67) and capturing a status of said instruction as it is executed, wherein said program is debugged in real time and while said program is executed ("the contents of the event history buffer can be recorded over time by the diagnostic device to provide a real time record of the processing events occurring in the chip during real time. This real time record taken together with knowledge of the program code being executed provides a true picture of the processors' execution sequence in real time and thereby expedite(s) debugging of code," col 3, lines 1-59; see also col 4, lines 51-67).

Regarding claim 54, Roy further discloses the step of restoring the original compiled code once the status is captured (col 2, lines 62-67; col 3, lines 3-32, lines 42-59).

Regarding claim 53, this claim is another version of the claimed method discussed in claims 54, wherein all claim limitations also have been addressed and/or covered in cited areas as set forth the above. To restore the original code once the status is captured as stated in claim 54, the step of returning to said compiled code in claim 53 is necessary and accordingly, this feature is inherent in Roy's disclosed method.

Regarding claim 55, Roy further discloses the step of instrumenting each instruction compiled in said another section of memory. Instrumentation is adding small code snippets at key points to existing code fragments to collect profiling information, to debug certain otherwise hard to solve faults, such as memory management issues and data races, or to analyze code which is loaded or even generated at run time. Roy discloses the method of instrumenting an instruction in column 4, lines 1-7, stating that "the contents of the cause register contain code which indicates an interrupt or exception...the instruction in IRAM pointed to by the program counter includes code indicating that it is a branch back to another instruction." See also col 3, lines 8-32, lines 19-32; col 4, lines 27-67; col 1, lines 35-40.

Regarding claim 56, Roy further discloses the step of storing a table relating instructions to boolean expressions, wherein said instructions are debugged with the boolean expressions ("the program branches to line 70 because the conditional expression of line 50 is true based on the variable D=7," col 5 26-67; "When line 50 is executed (now for the second time) the first decoder indicates that a program counter increment (INC) in the execution of the program has occurred and shows an output of "001" because the condition (D=7) for the jump in line 50 is no longer valid. Line 60 is now executed and a jump to a location stored in a register occurs." col 6, lines 1-38).

Regarding claim 57, Roy further discloses the step of providing a table of pointers to instructions of said original compiled code, wherein said instructions are located in memory during debugging ("Each program counter contains an index of the instructions in an associated IRAM and a pointer to the index as the instructions are executed by the processor. The cause registers store current information about interrupts, exceptions, and other processor functions," col 4, lines 15-20; see also col 4, lines 50-67; col 5, lines 1-25).

Regarding claim 58, Roy further discloses the step of limiting a data size of each compiled instruction, wherein execution of said instructions to be debugged is faster and memory required to store said instructions is reduced ("when the history buffer is enabled, it captures forty-four bits of information from the cause register or program counter," co 6, lines 40-67).

Regarding claims 59-62, they are the apparatus versions of claims 52, 56 and 57 respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 52, 56 and 57 above.

Response to Arguments

9. Applicant's arguments filed 3/10/2004 have been fully considered but they are not persuasive.

Per claims 52 and 59, the applicant simply states that neither Roy nor Logan discloses the limitations in the claims and fails to show why the limitations in the instant claims are different from the teachings of the references and that the reasons to combine and motivations concerning the rejections of claims are improper.

Per claim 52:

The applicant states in regards to claim 52 that:

> 1) Logan's debuggers' displaying of "a highlighted flowchart element" does not expressly or inherently teach or suggest the claimed "displaying a section of said program indicated by a user to be debugged."

In response to applicant's statement, Examiner points out that Logan discloses displaying a section of said program indicated by a user to be debugged ("the debugger...is supplied with data...in which when an interrupt is inputted via the keypad...providing data to the debugger to indicated which block or blocks are being executed at the time of interrupt. Inhibit signals come from the keyboard 92...The Debugger...drives **the display to highlight the particular block which was executing at the time of interrupt...The block numbers are displayed for purpose of enabling the programmer to get back into the flowchart at the required spot and highlights are utilized to indicate, during an interrupt cycle, which blocks in the program were executing at the time of the interrupt...only the flowcharts that are necessary to be edited will be called up to the display**," col 5 lines 25-col 6 lines 17) as claimed.

> 2) Logan does not expressly or inherently teach or suggest "compiling" a user-indicated section of a program" in another section of memory."

In response to applicant's statement, Examiner points out that Logan discloses compiling a user-indicated section of a program in another section of memory ("in which during an interrupt, the flowchart bocks may be highlighted by the aforementioned debugger...to correct whatever was the problem with the initial program. Thereafter, upon recompiling, the program...is executed ...with the simple editing having been accomplished through the addition of an additional set of blocks...displayed values may be changed in the debugger, and the displayed values executed without going through a complete recompile...the **debugger** allows the operator to isolate and

display the particular program blocks which were executing at the time of the interrupt and then re-edit the program though an **editor**...After the...changes have been made by the editor, they are **compiled by the compiler** and **loaded into the Executive program** so that the machine may be properly controlled," col 4 lines 1-56) as claimed.

> 3) Since Logan does not expressly or inherently teach or suggest "compiling" any "section" of the "program" in "another section of memory", Logan does not expressly or inherently teach or suggest "jumping to said another section of said memory."

In response to applicant's statement, Examiner points out that Logan discloses compiling a user-indicated section of a program in another section of memory as shown above. Therefore, accordingly, Logan inherently discloses jumping to another section of memory as claimed.

The applicant also states in regards to claim 52 that:

> Roy does not disclose "displaying a section of said program indicated by a user to be debugged."

In response to applicant's statement, Examiner points out that the applicant's argument is based on a single reference, Roy, not in combination with teachings by Logan. The applicant fails to show that the reasons to combine and motivations concerning the rejections of claim 52 are improper. Logan as shown above teaches displaying a section of said program indicated by a user to be debugged as claimed.

> Roy does not "expressly or inherently teach or suggest the claimed "compiling" a user-indicated "section" of a "program."

In response to applicant's statement, Examiner points out that in combination with teachings by Logan, Roy teaches compiling a user-indicated section of a program in another section of memory ("the contents of the history buffer...provide a relatively complete indication of each processor's execution sequence in real time...**a debugging system may be coupled to the...history buffer as illustrated**...When a bug is encountered, the complete history of instruction execution leading up to the failure can be reviewed...The debugging system is non-invasive and permits **debugging of programs operating in real time**," col 7 lines 20-55) as claimed.

> Since Roy does not expressly or inherently teach or suggest "compiling" any "section" of the "program" in "another section of memory", Roy does not expressly or inherently teach or suggest "jumping to said another section of said memory."

In response to applicant's statement, Examiner points out that Roy like Logan discloses compiling a user-indicated section of a program in another section of memory as shown above. Therefore, accordingly, Roy inherently discloses jumping to another section of memory as claimed.

As such, in view of the combined teachings by Logan and Roy, the rejection of claim 52 is proper and maintained.

Per claim 59:

The applicant states that neither Roy nor Logan, alone or combination, does not disclose the limitations of claim 52, for the similar reasons set forth in connection with claim 52. As shown

above, the rejection of claim 52 by the combined teachings of Roy and Logan is proper and maintained, and accordingly, the rejection of claim 59 is also maintained.

Per claims 53-58 and 60-62:

Regarding dependent claims 53-58 and 60-62, applicant fails to show why the limitations in the instant claims are different from the combined teachings of the references and that the reasons to combine and motivations concerning the rejections of claims 53-58 and 60-62 are improper. As has been shown above, the rejections of the independent claims 52 and 59 by Roy and Logan are proper and maintained. Accordingly, the rejections of claims 53-58 and 60-62 are also proper and maintained.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Insun Kang whose telephone number is 703-305-6465. The examiner can normally be reached on M-F 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on 703-305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IK
5/14/2004

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